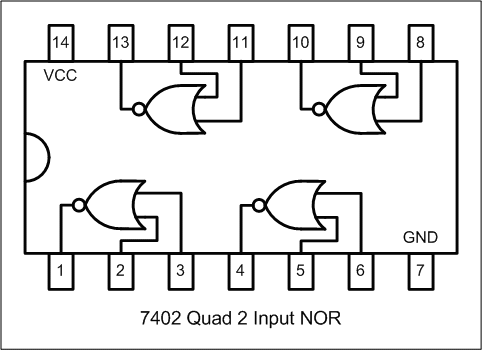
**Lab 5 Single NAND/NOR Chip Implementation**

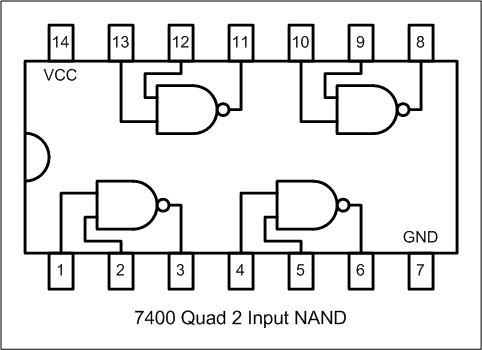
1. **Introduction**

NAND and NOR are universal gates and are preferred over AND or OR gates in logic design and chip fabrication. In this lab, the student will design, minimize and implement logic function using single NAND/NOR chip, i.e., you only need one chip on the board to build a circuit. Minimizing the number of chips can increase circuit reliability and reduce power consumption and system size.

1. **Components needed:** **note that 7402 chip has a different layout from 7400 chip.**

1 — 74HC**00** Quad 2-input NAND gate 1 — 74HC**02** Quad 2-input NOR gate





1. **All NAND Gate Implementation**

You are to build a circuit to implement the following function:

**F = AB + BC’**

1. Derive the truth table for the function, and draw the logic diagram using AND, OR and NOT gates:

|  |  |  |  |
| --- | --- | --- | --- |
| A B C | AB | BC’ | F |
| 0 0 0 | 0 | 0 | 0 |
| 0 0 1 | 0 | 0 | 0 |
| 0 1 0 | 0 | 1 | 1 |
| 0 1 1 | 0 | 0 | 0 |
| 1 0 0 | 0 | 0 | 0 |
| 1 0 1 | 0 | 0 | 0 |
| 1 1 0 | 1 | 1 | 1 |
| 1 1 1 | 1 | 0 | 1 |

1. Convert the circuit diagram to **all NAND gates implementation.**

**Diagram

Description automatically generated**

1. Circuit construction on Tinkercad (DO NOT tear down the circuit after you finished this step.)

Based on the diagram in (b), build the circuit using one **7400** chip. DIP switches will be used to supply all three input logic levels A, B and C, and a LED will be used to provide the F output.

1. Make a copy of the starter kit from <https://www.tinkercad.com/things/19XqriP2dMF> and rename the copy as “Lab 5 Single Chip Implementation” on Tinkercad Circuits dashboard.
2. Connect the NAND gates according to the logic diagram from Step (b).
3. Connect the inputs (A, B, C) to three switches, and the output F to a LED.
4. Press “Start Simulation”.
5. Apply all eight combinations of logic LOW and HIGH levels to the three gate inputs using the DIP switches. Observe if the circuit outputs match the values in the truth table.
6. **All NOR Gate Implementation**
7. Rewrite the function as the Product of Sums format
   * 1. **F = AB + BC’ = B(A+C’)**
8. Draw the logic diagram using AND, OR and NOT gates:

Diagram

Description automatically generated

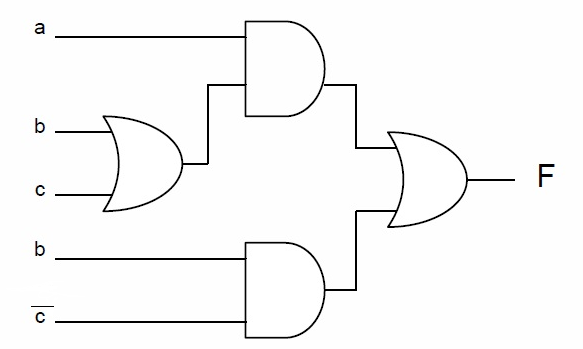
1. Convert the circuit diagram to **all NOR gates implementation.**

**Diagram

Description automatically generated**

1. On Tinkercad, place a **7402** chip on the breadboard and build the circuit using the diagram (c). **Note that 7402 chip has a different layout from 7400 chip.**
2. Connect the NOR gates according to the logic diagram.
3. Connect the inputs (A, B, C) to three switches, and the output F to a LED.
4. Press “Start Simulation”.
5. Apply all eight combinations of logic LOW and HIGH levels to the three gate inputs using the DIP switches. Observe if the circuit outputs match the values in the truth table.
6. **Homework**: Draw the equivalent purely NAND/NOR gate representation of the function below and build the circuits on Tinkercad using NAND and NORchips, respectively. **DO NOT simplify the function or change the fuction to sum-of-product or product-of-sum format!**  In the lab report, include the logic diagram with NAND implementation, the diagram with NOR implementation, the Tinkercad screenshot and link.







F = a(b + c) + bc’



**Submission Instructions:**

Lab work submission

1. Take screenshots of your circuits with eight input combinations.
2. Copy the link of your circuits for sharing.
3. On the Blackboard, click on Lab 5. Attach the screenshot from Step 1 and paste the link from Step 2 into the Comments area, then hit the Submit button.

Lab report submission

1. Lab report is needed for this lab. Please follow the guidelines and sample report on the Blackboard when you are writing your lab reports. Click on **Lab 5 Report Submission** to submit your report. It is due one week after the lab is done.

0 0 0 = 0

Diagram

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0 0 1 = 0

Diagram

Description automatically generated

0 1 0 = 1

Diagram

Description automatically generated

0 1 1 = 0

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1 0 0 = 0

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